

WHAT IS CLAIMED IS:

1. A semiconductor memory comprising:

a plurality of memory cell arrays constituted of
a plurality of memory cells or memory cell units which
5 consists of a plurality of memory cells, arranged in
a matrix,

wherein the plurality of memory cell arrays
constitute a plurality of cell array groups each of
which consists of two or more memory cell arrays, and
10 a first Pass/Fail signal indicative of success or
failure of an operation is outputted in accordance with
each cell array group.

2. The semiconductor memory according to claim 1,
wherein the operation includes a parallel operation
15 with respect to memory cells in two or more of the
plurality of cell array groups.

3. The semiconductor memory according to claim 1,
wherein the operation includes a parallel operation
with respect to memory cells in two or more of the
20 plurality of cell arrays.

4. The semiconductor memory according to claim 1,
wherein the operation is a program or an erase
operation.

5. The semiconductor memory according to claim 1,
25 wherein the first Pass/Fail signal is a Pass/Fail
signal indicating whether the operation has attained
success with respect to all of selected memory cells

included in each of the cell array groups or not.

6. The semiconductor memory according to claim 1,
wherein a second Pass/Fail signal of an entire chip is
also outputted when the first Pass/Fail signal is
5 outputted.

7. The semiconductor memory according to claim 1,
wherein the first Pass/Fail signal is a Pass/Fail
signal indicating whether the operation has attained
success with respect to one memory cell array selected
10 from the two or more memory cell arrays in each of the
cell array groups or not.

8. The semiconductor memory according to claim 1,
wherein the first Pass/Fail signal is outputted after
a first command is inputted.

9. The semiconductor memory according to claim 8,
wherein the first Pass/Fail signal is not outputted and
a third Pass/Fail signal which is different from the
first Pass/Fail signal is outputted after a second
command is inputted.

10. The semiconductor memory according to claim 8,
wherein a forth Pass/Fail signal is outputted with
respect to each of the cell arrays included in an
entire chip after a third command is input.

11. The semiconductor memory according to
25 claim 10, wherein the third command is different from
the first command.

12. The semiconductor memory according to claim 1,

wherein the memory cell is EEPROM.

13. The semiconductor memory according to claim 1,
wherein the memory cell unit is a NAND cell type
EEPROM.